DISTRIBUTED ANALYSIS OF SUBMICRON-MESFET NOISE-PROPERTIES

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ABSTRACT

A distributed MESFET noise-analysis is presented. Its results are used to determine the validity range of common lumped-element models. We found that in well-designed submicron LN-MESFETs distributed effects may be neglected. Practical gate-width design-values are given.

INTRODUCTION

State-of-the-art low-noise MESFETs show transit frequencies of more than 100 GHz at submicron gate-lengths (e.g. (1)). FET modelling, on the other hand, did not keep pace with this rapid development due to both problems in device measurement techniques and a lack of basic theoretical work studying the frequency range above 20 GHz.

As well known, when increasing frequency, the device dimensions have to be reduced in order to maintain the desired lumped-element characteristics. Scaling down the unit gate-width W, however, one encounters difficulties, since the wave length in FETs ranges around 1/10 of its free-space value and inherent physical laws such as power density limitations put lower-bound restrictions on W. Recently, several papers treated this problem indicating that distributed effects may affect the FET high-frequency behaviour (e.g.: Pucel (2), Ghione et al. (3)).

Therefore, the question arises whether the common lumped-element models hold further on or whether novel distributed models are required. As a consequence, a distributed analysis has to be employed that takes into account the wave propagation along the gate-width direction. This is presented here, studying both signal and noise properties of submicrometer-gate MESFETs. Naturally, such a treatment can be used not only to investigate the limits of present lumped-element models but also to develop novel FET structures taking advantage of the wave-propagation phenomena.

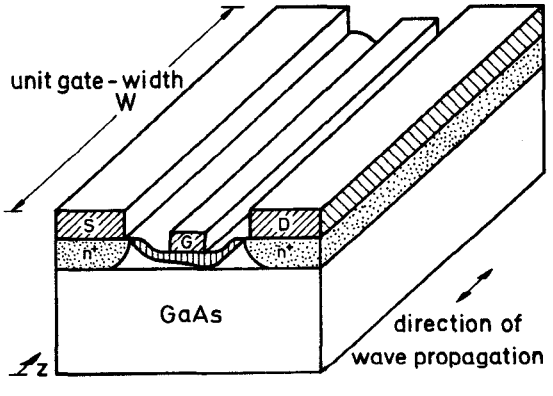

Fig. 1 Elementary FET cell of unit width W

METHOD OF ANALYSIS

In order to cover the various electrode peripheries in use we consider an elementary FET of unit gate-width W (see Fig. 1). Depending on the actual geometry two different input-output configurations have to be distinguished, namely (see Fig. 2): Input and output are located at opposite ends of the transistor or at one side.

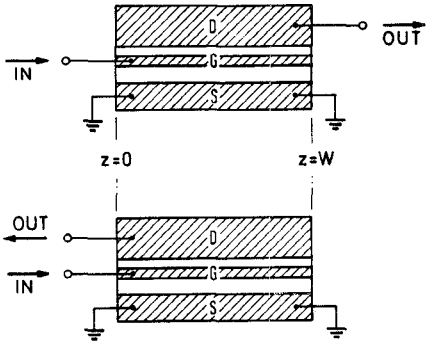

Fig. 2 The two input-output configurations

The treatment presented in the following is based on fundamental field-theoretical work on MESFET wave-propagation, which clearly suggests that the relevant wave modes are quasi-TEM ones (see (4)). Consequently, a suitable distributed

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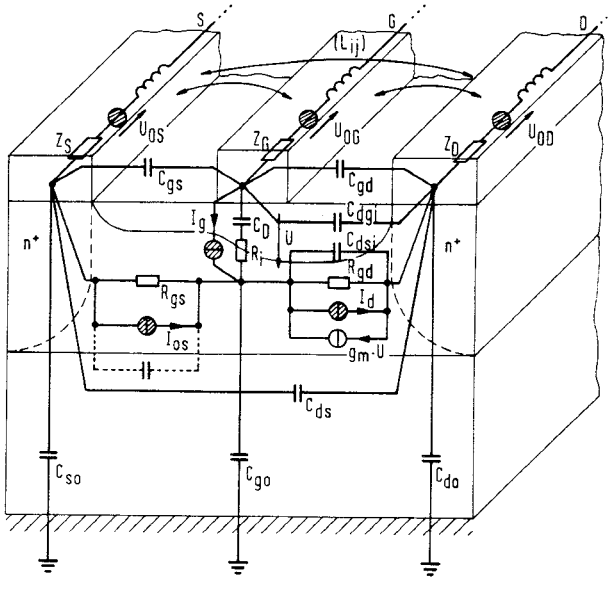
equivalent-circuit description holds well as demonstrated in (5). This latter model has now been extended (see Fig. 3):

Firstly, the full small-signal equivalent circuit is incorporated and, secondly, the FET noise-sources are included.

Assuming 0.25µ gate-length we chose the parameters according to measurement-fitted values taken from the literature or, if not available, from recent theoretical work (6,7).



$$g_m = \frac{g_{mo}}{1+j\omega\tau_{t2}} \, e^{-j\omega\tau_{t1}}$$

$U_{OS}, U_{OG}, U_{OD}, I_{OS}$ - thermal noise sources

$$\langle I_g \cdot I_g^* \rangle = 4kT\Delta f \cdot \frac{\omega^2 C_D^2}{g_{mo}} \cdot R$$

$$\langle I_d \cdot I_d^* \rangle = 4kT\Delta f \cdot g_{mo} \cdot P$$

$$\langle I_g^* \cdot I_d \rangle = 4kT\Delta f \cdot \omega C_D \cdot C_{cor} \sqrt{RP}$$

Fig. 3 The small-signal FET model (all elements are distributed ones)

A detailed description of the distributed noise analysis would exceed the scope of this paper. Fig. 4 explains the procedure on principle:

We consider a noisy FET subsection of differential gate width Δz, which, for $\Delta z \to 0$ may be described by means of usual lumped theory. Assuming the remaining transistor sections to behave noiseless but distributed, the corresponding noise currents at the ports on both FET sides can be calculated.

According to common theory (e.g. (8)) the noise generated by different FET sections is uncorrelated. Hence, superposing the contributions of all differential sections gives the total noise port-representation. It should be outlined that no additional physical assumptions are required compared with previous lumped treatments (7,8). Concerning the description of noise behaviour itself, the representation by correlation matrices (9) proved to be very useful.

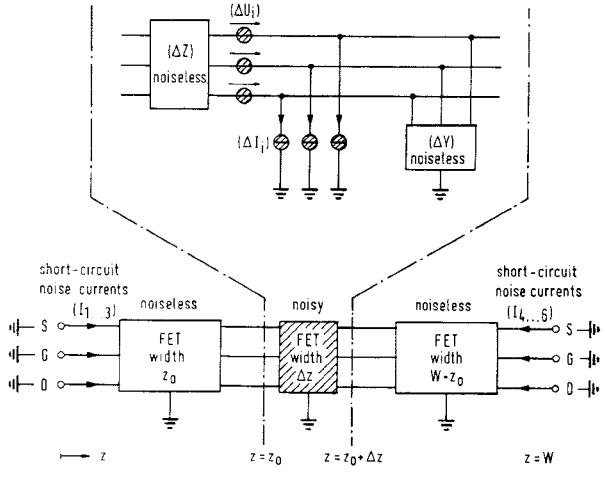


Fig. 4 Distributed analysis of FET noise: Contributions by noisy subsection of differential gate-width Δz

The results from distributed analysis are then compared to the corresponding lumped-element formulation as depicted in Fig. 5. Note that the usual FET equivalent-circuit neglects any mutual inductances between the electrodes.

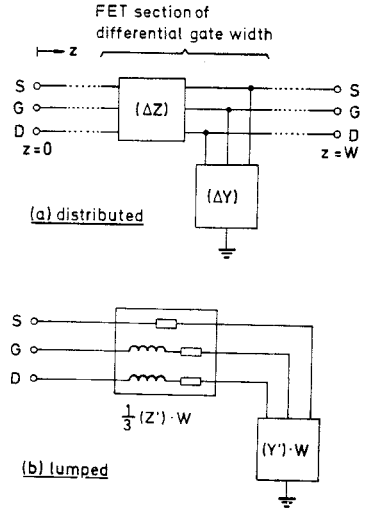


Fig. 5 Matrix description of the distributed and the corresponding lumped-element model

RESULTS

Fig. 6 illustrates the behaviour of gain and minimum noise figure when increasing the unit gate-width. Obviously, the onset of gain and noise-figure degradation occures at gate widths smaller than the limit where deviations due to distributed effects become remarkable!
That means with regard to low-noise applications: Because one ought to choose the unit gate-width small enough in order to avoid noise-figure deterioration, lumped-element modelling may be adopted in such cases.

More systematically, we compared the corresponding scattering coefficients (S) and noise-correlation matrices (C) and calculated the resulting maximum percentual element-deviation (weighted by the row maximum). Assuming a fixed error bound (e.g. 5%) one then obtains detailed information on the validity range of the lumped model. Similarly, the NFmin and gain degradation with growing width W dictate limitations. Tolerating a maximum associated-gain decrease of 1 db and a NFmin increase of 0.5 db we achieve an upper bound for W, too.

Fig. 7 presents these different limitations graphically. The indices "O" and "W" refer to the different input-output configurations (output at z=0 and z=W, respectively - see Fig. 2). The corresponding deviations, however, are of no significance with regard to the following considerations.

CONCLUSIONS

From the results derived above one concludes that distributed effects can be neglected in conventional submicron LN-MESFETs with well-designed unit gate-width. A systematic investigation varying the equivalent-circuit elements within their realistic range confirmed this finding.

In special cases, however, the inductive coupling between gate and drain electrodes has to be included to maintain the given accuracy at frequencies beyond about 40 GHz.

In general, the off-diagonal elements $(C)_{12}$ and $(C)_{21}$ of the noise-correlation matrix dominate the errors (note that $(C)_{12}$ is the complex conjugate of $(C)_{21}$ - see (9)).
Hence, distributed effects influence the correlation between the equivalent input and output noise sources in the first place. This causes reduced noise cancellation and thus increased NFmin (see Fig. 6).

The results point out the importance of unit gate-width to FET-design. Proper values for W avoiding excessive deterioration of the LN-performance may be seen from Fig. 7.

Finally, it should be noted that the analysis presented here can be applied to HEMT devices without further modifications. Merely, adequate element values for the equivalent circuit have to be employed.

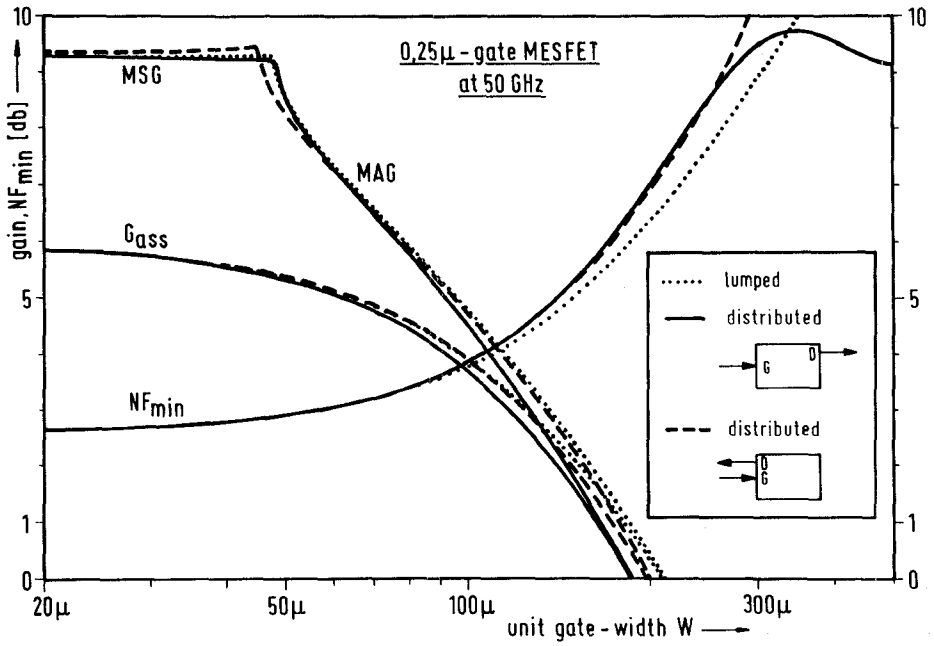
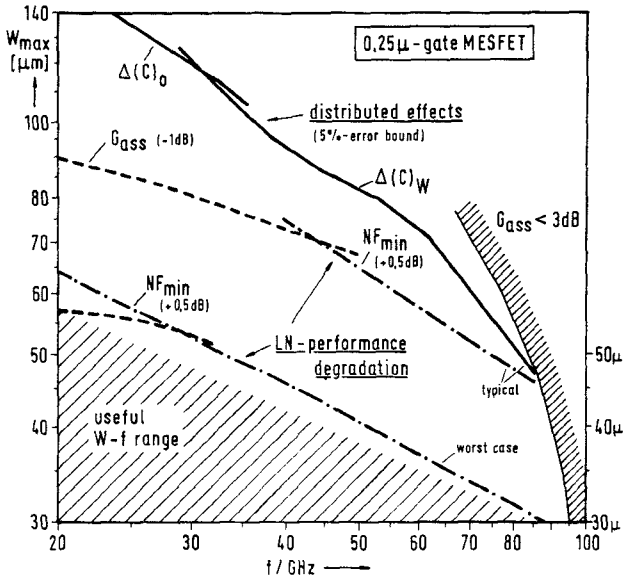


Fig. 6 Minimum noise figure and gain against unit gate-width
(Comparison between lumped modelling and distributed analysis applying the two different input-output configurations as indicated)



W_{max} - Maximum unit gate-width due to the following limitations:

——— The maximum percentual element error of the correlation matrix (C) due to distributed effects exceeds 5% (the indices "0" and "W" denote the two possible input-output configurations of Fig. 2)

— — — G_{ass} degradates more than 1 db

—·—·— NF_{min} increases more than 0.5 db

Fig. 7 Maximum unit gate-width as a function of frequency for a typical 0.25µ-gate MESFET

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